Notice of Allowability	Application No.	Applicant(s)	
	10/659,892	KUEKES ET AL.	
	Examiner	Art Unit	
	Guy J. Lamarre	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *8/25/06*.

2. ☒ The allowed claim(s) is/are *1-37*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Guy J. Lamarre, P.E
Primary Examiner

Reasons For Allowance

1. **Claims 1-37** are allowable over the prior art.

1.1 The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art is exemplified by (US Patent No. 7073157) to **DeHon et al.**

DeHon et al discloses, e.g., in Figs. 6-7, nanoelectronics/microelectronics interfacing comprising address line encoding for signal differentiation, e.g., *'The architecture according to the present invention is based on a plurality of array cells. Therefore, power supply gating crossbars acting as decoders will be needed to allow a small number of microscale wires to connect to a larger number of nanoscale wires forming the array grids. In particular, the crossbars will have a set of crossed nanoscale wires. A first set of the nanoscale wires will be connected to a power supply and a second, orthogonal, set of nanoscale wires will control the resistance along the first set of wires. FIG. 6 shows a nanoscale decoder block 60 on the edge of a nanowire array, not shown in the Figure. The decoder has N nanowires 64 (four in the figure) which connect to the nanowire array and 2 log.sub.2(N)+1 nanowires 65 (five in the figure) which connect to an orthogonal set of microscale wires 62 through nanovias 63. The extra control line 66 (the +1 in wires 65) is an enable line used to enable/disable the decoder connection. As usual, black squares in the decoder show OFF positions, allowing a unique address to be assigned to each of the nanoscale wires 64 of the decoder. FIG. 6 also shows a horizontal microscale wire 61 connected to the supply voltage. The microscale wire 61 is a source for the driving voltages in the array, i.e. one of the power supply lines for the circuit. However, while address lines which are connected directly to the microscale wires 62 can be driven to a voltage by conventional electronics, it is not possible to drive the nanoscale wires 64 which drive into the nanowire array. To address this, the decoder pattern can be customized during fabrication. An example of this customization in shown in FIG. 7, where a customized decoder 60 is shown, obtained through a stamping process...In particular, a predetermined pattern of blocks between the orthogonal layers of wires connecting to the nanowire array and to the microscale wires is imprinted. Where the pattern leaves openings, the two layers are allowed*

to contact, producing a strongly coupled FET arrangement. See, for example, location 70 in FIG. 7. Where the blocks prevent the crossed wires from contacting, the crossed nanowires are far enough apart that they do not control each other. In a preferred embodiment, sparse encoding will be used, i.e. the decoder will be provided with additional encoding lines, in order to guarantee that a faulty address line will still allow proper operation of the decoder or will render only a small fraction of the array unaccessible. For example, a two-hot coding scheme can be considered, where every nanowire 64 is enabled by ANDing together a pair of address wires. Therefore, the patterning of the decoder does not need to be perfect, because it will always be possible, in the preferred embodiment, to tolerate not being able to address a small fraction of the nanoscale wires.'

However, DeHon et al does not teach or suggest the combination of claim elements as described in **Claims 1-37**.

1.2 Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

* Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (571) 273-8300 for all formal communications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (571) 272-3826. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached at (571) 272-3819.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-3609.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Guy J. Lamarre, P.E
Primary Examiner
11/12/2006